

Electronic Acknowledgement Receipt

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International Application Number:	
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Title of Invention:	A SYSTEM AND METHOD OF PROVIDING ERROR DETECTION AND CORRECTION CAPABILITY IN AN INTEGRATED CIRCUIT USING REDUNDANT LOGIC CELLS OF AN EMBEDDED FPGA
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		BUR920040001US1_Respo nsetoRestrictionRequirement .pdf	75156 00f7ab87898efa2665c1dca3b4933a72 66078964	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Response to Election / Restriction Filed	1	3
	Miscellaneous Incoming Letter	4	4
Warnings:			
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